Electronic Version
Stylesheet Version v1.1.1

INTEGRATED CIRCUIT

Abstract

A plurality of decoding circuits 1a to 1f are arranged near a plurality of circuit blocks 2 to 7, which are arranged on the semiconductor chip 10 in a scattered manner, and the signal lines 8 prior to decoding, including the address lines and the data lines, are wired to each decoding circuit 1a to 1f. Through these wirings, the number of wirings routed over on the semiconductor chip 10 can be made in accordance with the number of bits of the signal lines 8 alone. So, compared with the past where the signal lines 20, which were great in number after decoding, were routed over to each circuit block 2 to 7, the wiring area as a whole can be greatly reduced. This can lead to miniaturization of chip size, reduction of crosstalk noise, and facilitation of layout.